

## SEMICONDUCTOR DEVICE

CROSS REFERENCE TO RELATED APPLICATION

This application claims benefit of priority under 35 U.S.C.  
5 § 119 to Japanese Patent Applications No. 2002-213331, filed on  
July 23, 2002, and No. 2002-295629, filed on October 9, 2002,  
the entire contents of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION10 Field of the Invention

The present invention relates to a semiconductor device  
to which a semiconductor chip having a cell such as a MOS-type  
power device is incorporated.

15 Related Art

In recent years, scale-down is demanded from a power device  
such as a vertical MOSFET, and a reduction in the value of internal  
resistance (on-state resistance or the like) of the entire  
semiconductor device including the aforementioned device is also  
20 strongly demanded. Fig. 20 shows an example of a related  
semiconductor device. Here, 2001 denotes a semiconductor  
substrate, 2002 denotes a source electrode, 2003 denotes a lead  
frame, 2004 denotes a source wire, 2005 denotes a gate wire, and  
2006 denotes a gate wiring.

25 A lead-out wiring region and a cell forming region are  
provided on the surface of a semiconductor chip, and a cell such  
as a MOSFET is formed in the cell forming region. The source  
electrode 2002 and the lead frame 2003 are connected by a plurality  
of source wires 2004. The source electrode is required to pass  
30 more current than a gate electrode, but since it is connected  
by the wires, the cross-sectional area of a current path is small,  
and hence the resistance value is high. To reduce this resistance  
value, there is a technique in which a reduction in on-state  
resistance is achieved by a structure in which the source electrode  
35 and the lead frame are connected by an almost platy conductive  
plate. Hereinafter, this almost platy conductive plate is called  
a strap. Moreover, the structure in which the source electrode

and the lead frame are connected by the strap is called a strap structure. For example, in Japanese Patent Laid-open No. 2000-114445, a method of connecting a Cu strap onto an electrode on the surface of a semiconductor chip by an Ag paste as an adhesive  
 5 is disclosed.

This method has the following problem depending on conditions. Namely, if a temperature cycling test, one of common reliability tests of a semiconductor device, in which the semiconductor device is disposed under an environment with a wide  
 10 range of temperature and a sharp temperature change, is repeated a plurality of times, there arises a problem that a fault such as cracking occurs in the vicinity of an interface since thermal efficient coefficients of an electrode member, the adhesive, and the strap are different from one another, whereby the life of  
 15 the semiconductor device is shortened.

As a technique to solve this problem, a method of directly connecting the strap to the electrode on the surface of the semiconductor chip by ultrasonic bonding is newly proposed. Fig. 21 is a fragmentary sectional view of a related semiconductor  
 20 device and shows a lead-out wiring region including a gate wiring and the like. It shows a region corresponding to the line A-A' in Fig. 20, and it is a sectional view of a first lead-out wiring region sandwiched between source electrodes out of the lead-out wiring region. A device such as a MOSFET is formed in another  
 25 cell forming region, and an N-type source region (not shown) is selectively formed on the surface of a P-type base region 2102 formed on a semiconductor substrate 2101. A first insulating film 2103 is formed on the P-type base region 2102. A first gate wiring 2104 is formed on part of the first insulating film 2103, and  
 30 the first gate wiring 2104 is connected to a gate electrode (not shown) such as the MOSFET formed in another cell forming region.

A first interlayer dielectric 2106 is formed on a side surface and part of an upper surface of the first gate wiring 2104 for insulation from a source electrode 2105. A second gate wiring  
 35 2107 made of Al (Aluminum) is formed on the upper surface of the first gate wiring 2104 on which the first interlayer dielectric 2106 is not formed. The source electrode 2105 is formed on the

P-type base region 2102 and the N-type source region. An upper surface of the second gate wiring 2107 is formed higher than an upper surface of the source electrode 2105. A protective film 2108 such as polyimide is formed on part of the source electrode 2105 and on the second gate wiring 2107. The protective film 2108 is formed in order to prevent a short-circuit between the second gate wiring 2107 and a strap formed thereabove, a short-circuit between the second gate wiring 2107 and the source electrode 2105, corrosion of Al, and the like. The source electrode 2105 is connected to a strap 2109 by ultrasonic bonding.

Fig. 22 is a fragmentary sectional view of the related semiconductor device and shows another lead-out wiring region including the gate wiring and the like. It is a sectional view of a region corresponding to the line B-B' in Fig. 20 and shows an outer peripheral region of the cell forming region out of the lead-out wiring region. It is a sectional view of a second lead-out wiring region in which a gate electrode and the lead frame are connected by the gate wire.

A first insulating film 2202 is formed on a semiconductor substrate 2201. A first gate wiring 2203 is formed on part of the first insulating film 2202, and a first interlayer dielectric 2204 is formed on a side surface and part of an upper surface of the first gate wiring 2203. A second gate wiring 2205 made of Al is formed on the upper surface of the first gate wiring 2203 on which the first interlayer dielectric 2204 is not formed, and an end portion of the second gate wiring 2205 is formed to extend onto the first insulating film 2202. A wiring portion which extends onto the first insulating film 2202 is used as a gate electrode 2207. A source electrode 2206 is formed apart from the gate electrode 2207, and a protective film 2208 such as polyimide is formed on part of the source electrode 2206 and on part of the gate electrode 2207 in order to prevent a short-circuit between the gate electrode 2207 and the source electrode 2206 and corrosion of Al. The source electrode 2206 is connected to the strap by ultrasonic bonding, and the gate electrode 2207 is connected to the gate wire (not shown). A stopper region 2209 is formed in a surface region of an outer peripheral edge of the semiconductor

substrate 2201.

Fig. 23 to Fig. 25 show a method of manufacturing a semiconductor device in the first and second lead-out wiring regions shown in Fig. 21 and Fig. 22. The cell forming region is omitted.

As shown in Fig. 23, a P-type base region 2302 is formed on a semiconductor substrate 2301 in the first lead-out wiring region. Subsequently, first insulating films 2303a and 2303b are formed on the P-type base region 2302 and the semiconductor substrate 2301 of the first and second lead-out wiring regions, respectively. Polysilicon is deposited on the first insulating films 2303a and 2303b and etched to form first gate wirings 2304a and 2304b on part of each of the first insulating films 2303a and 2303b in the first and second lead-out wiring regions. Silicon nitride films are formed on upper surfaces and side surfaces of the first gate wirings 2304a and 2304b and etched to form first interlayer dielectrics 2305a and 2305b having slot portions such that part of each of the upper surfaces of the first gate wirings 2304a and 2304b is exposed.

Then, Al is deposited and etched to form a second gate wiring 2306a in the first lead-out wiring region and a gate electrode 2307 integrated with a second gate wiring 2306b in the second lead-out wiring region. A source electrode 2308 is formed in the cell forming region (only part of the source electrode is shown). The gate electrode 2307 formed in the second lead-out wiring region is formed on the first insulating film 2303b. The source electrode 2308 is formed apart from the second gate wiring 2306a and the gate electrode 2307. A stopper region 2309 is formed in a surface region of an outer peripheral edge of the second lead-out wiring region.

Next, as shown in Fig. 24, polyimide 2310 is deposited in the first and second lead-out wiring regions.

Thereafter, by applying a resist film and forming a resist pattern, a protective film such as covers the gate wiring and a protective film 2311 such that part of the upper surface of the gate electrode is exposed are formed as shown in Fig. 25. Subsequently, the strap (not shown) is formed on the cell forming

region and the first lead-out wiring region, and the gate wire (not shown) is formed on the gate electrode 2307 formed in the second lead-out wiring region and connected to the lead frame.

However, reliability to heat increases dramatically in ultrasonic bonding, but since the strap is bonded by applying ultrasonic waves to a predetermined region of the strap, if the ultrasonic waves are applied to a region on the projecting gate wiring in the first lead-out wiring region, a large shock is applied to the protective film on the gate wiring. Consequently, the projecting gate wiring is crushed, and the gate wiring and the source electrode are deformed, which causes a problem that a short-circuit between the gate wiring and the source electrode occurs, or the protective film formed on the gate wiring deteriorates to cause a short-circuit between the strap and the gate wiring. The aforementioned problem does not arise unless the projecting upper-layer gate wiring with low resistance is formed in the upper portion, but there is a problem that the existence of the upper-layer gate wiring exerts a large influence on internal resistance, and if the upper-layer gate wiring is not formed, for example, a resistance value of approximately 1.5  $\Omega$  increases to 3  $\Omega$  which is almost twice. In a power MOSFET especially used for synchronous rectification in recent years, an increase in resistance value lowers conversion efficiency, and hence it is not suitable for this use.

#### SUMMARY OF THE INVENTION

In order to accomplish the aforementioned and other objects, according to one aspect of the present invention, a semiconductor device, comprises

a semiconductor layer which includes a first semiconductor region of a first conductivity type, a base region of a second conductivity type, and a plurality of second semiconductor regions of the first conductivity type;

a gate wiring which is formed on the semiconductor layer via a first insulating film;

a plurality of main electrodes which are electrically connected to the plurality of second semiconductor regions and

which are insulated from the gate wiring, wherein the gate wiring is arranged between the main electrodes and upper surfaces of the main electrodes are higher than an upper surface of the uppermost layer of the gate wiring; and

- 5           a connecting plate which is directly connected onto uppermost layers of the main electrodes.

According to another aspect of the present invention, a semiconductor device, comprises:

- 10           a semiconductor layer which includes a first semiconductor region of a first conductivity type, a base region of a second conductivity type, and a cell forming region in which a plurality of second semiconductor regions of the first conductivity type are formed;

- 15           a first gate electrode which is formed in the cell forming region and controls continuity/non-continuity between the first semiconductor region and the second semiconductor region;

- 20           a plurality of main electrodes which are electrically connected to the plurality of second semiconductor regions respectively and which are formed at predetermined intervals in the cell forming region on the semiconductor layer;

- 25           a gate wiring which is formed on the semiconductor layer between the plurality of main electrodes via a first insulating film and which leads out the first gate electrode to an outer peripheral region of the cell forming region, wherein upper surfaces of the uppermost layers of the plurality of main electrodes are higher than an upper surface of the uppermost layer of the gate wiring; and

          a first connecting plate which is directly connected onto the plurality of main electrodes.

- 30           According to a further aspect of the present invention, a semiconductor device, comprises:

          a first semiconductor layer of a first conductivity type;  
          a second semiconductor layer of a second conductivity type which is formed on the first semiconductor layer;

- 35           a first semiconductor region of the first conductivity type which is formed in a first cell forming region in the second semiconductor layer;

a second semiconductor region of the first conductivity type which is formed in a second cell forming region in the second semiconductor layer;

5 a first gate electrode which is formed in the first cell forming region and controls continuity/non-continuity between the first semiconductor region and the first semiconductor layer;

a second gate electrode which is formed in the second cell forming region and controls continuity/non-continuity between the second semiconductor region and the first semiconductor layer;

10 a first main electrode which is electrically connected to the first semiconductor region and formed in the first cell forming region on the second semiconductor layer;

a second main electrode which is electrically connected to the second semiconductor region and formed in the second cell forming region on the second semiconductor layer;

15 a gate wiring which is formed on the second semiconductor layer between the first main electrode and the second main electrode via a first insulating film and which leads out the first and second gate electrodes to an outer peripheral region of the first and second cell forming regions, wherein an upper surface of the uppermost layer of the first main electrode and an upper surface of the uppermost layer of the second main electrode are higher than an upper surface of the uppermost layer of the gate wiring; and

25 a first connecting plate which is directly connected onto the first main electrode and the second main electrode.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a fragmentary sectional view taken along the line A-A' of a semiconductor device in Fig. 8 according to a first embodiment;

Fig. 2 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the first embodiment;

35 Fig. 3 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the first embodiment;

Fig. 4 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the first embodiment;

Fig. 5 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the first embodiment;

Fig. 6 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the first embodiment;

Fig. 7 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the first embodiment;

Fig. 8 is a plan view of the semiconductor device according to the first embodiment;

Fig. 9 is a fragmentary sectional view taken along the line C-C' of each of semiconductor devices in Fig. 8 and Fig. 16 according to the first embodiment and a third embodiment;

Fig. 10 is a fragmentary sectional view of a semiconductor device according to a second embodiment;

Fig. 11 is a fragmentary sectional view taken along the line A-A' - B-B' of the semiconductor device in Fig. 16 according to the third embodiment;

Fig. 12 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the third embodiment;

Fig. 13 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the third embodiment;

Fig. 14 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the third embodiment;

Fig. 15 is a fragmentary sectional view showing one step of the process of manufacturing the semiconductor device according to the third embodiment;

Fig. 16 is a plan view of the semiconductor device according to the third embodiment;

Fig. 17 is a diagram showing a layout of the semiconductor



device according to the third embodiment;

Fig. 18A and Fig. 18B are diagrams showing other layouts of the semiconductor device according to the third embodiment;

Fig. 19 is a fragmentary sectional view of another  
5 semiconductor device according to the third embodiment;

Fig. 20 is a plan view of a related semiconductor device;

Fig. 21 is a fragmentary sectional view of the related semiconductor device;

Fig. 22 is another fragmentary sectional view of the related  
10 semiconductor device;

Fig. 23 is a fragmentary sectional view showing one step of the process of manufacturing the related semiconductor device;

Fig. 24 is a fragmentary sectional view showing one step of the process of manufacturing the related semiconductor device;

Fig. 25 is a fragmentary sectional view showing one step  
15 of the process of manufacturing the related semiconductor device;  
and

Fig. 26A and Fig. 26B are diagrams showing examples of a layout of the related semiconductor device.

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#### DETAILED DESCRIPTION OF THE EMBODIMENTS

Embodiments will be described in detail below.

(First Embodiment)

First, a semiconductor device of the first embodiment will  
25 be explained with reference to Fig. 1 to Fig. 8.

In this embodiment, the explanation is given with a MOSFET and an IGBT as its examples. Fig. 1 is a sectional view taken along the line A-A' in Fig. 8. As shown in Fig. 1, a first insulating film 103 is formed, for example, on a P-type base region 102 of  
30 a lead-out wiring region which is formed on an N-type semiconductor substrate 101 and sandwiched between cell forming regions. A first gate wiring 104 is formed on the first insulating film 103.

A trench 105 is formed perpendicular and parallel to the first gate wiring 104 in the P-type base region 102 of the cell forming region. The trench 105 has an offset mesh trench structure. Incidentally, Fig. 1 is a fragmentary sectional view of a region  
35 in which the trench 105 is formed parallel to the first gate wiring

104. A gate insulating film 106 is formed in the trench 105, and a trench gate electrode 107 is buried in the trench 105 in such a manner as to touch the gate insulating film 106. An N-type source region 108 is formed on the surface of the P-type base region 102 around the trench 105. The N-type source region 108 is not formed around the trench 105 on the lead-out wiring region side.

A cell formed in the cell forming region functions as a MOSFET if an N<sup>+</sup>-type drain region is formed under the semiconductor substrate 101 and a drain electrode is formed so as to touch the N<sup>+</sup>-type drain region, and functions as an IGBT (Insulated Gate Bipolar Transistor) if a P<sup>+</sup>-type collector region is formed under the semiconductor substrate 101 and a collector electrode is formed so as to touch the P<sup>+</sup>-type collector region. The cell formed in the cell forming region is not limited to the above. The structure of the cell is not limited to a trench type, and may be a planer type.

The first gate wiring 104 and the trench gate electrode 107 are formed of a conductive material such as polysilicon and electrically connected to each other in another region (not shown).

A first interlayer dielectric 109 such as a UDO (Undoped Oxide) or a BPSG is formed on a side surface and part of an upper surface of the first gate wiring 104. On the first gate wiring 104 on which the first interlayer dielectric 109 is not formed, a second gate wiring 110 formed of a conductive material such as Al is formed and used as a lead-out wiring for the first gate wiring 104 and the trench gate electrode 107. The first insulating film 103 and the first interlayer dielectric 109 may be integrally formed by an insulating film made of the same material. A second interlayer dielectric 111 is formed on the trench gate electrode 107. The second interlayer dielectric 111 may be completely buried in the trench 105.

A first source electrode 112 such as Al is formed on the P-type base region 102 and the N-type source region 108. The first source electrode 112 is formed so as to have a large area, which leads to a reduction in resistance. The first source electrode 112 is formed to be insulated from the first gate wiring 104 by the first interlayer dielectric 109 and insulated from the trench

gate 107 by the second interlayer dielectric 111. On part of an upper surface of the first source electrode 112 and a side surface and an upper surface of the second gate wiring 110, a second insulating film 113 is formed in order to, when an almost platy  
5 connecting plate (here called a strap) is connected by ultrasonic bonding, prevent a short-circuit between the second gate wiring 110 and the strap and a short-circuit between the first source electrode 112 and the second gate wiring 110.

Although the second insulating film 113 is also formed on  
10 part of the upper surface of the first source electrode 112, it may not be formed thereon. However, by forming the insulating film to extend onto part of the upper surface of the first source electrode 112 as described above, a short-circuit fault caused by misalignment in patterning can be prevented, whereby a device  
15 with high yield and high reliability can be manufactured. The second insulating film 113 is composed of a silicon oxide film, a silicon nitride film, or a stacked film thereof. It is desirable to use an insulating film with a certain degree of hardness as the second insulating film 113 since an electrode layer is formed  
20 thereon. The thickness of the second insulating film 113 is preferably 2  $\mu\text{m}$  to 4  $\mu\text{m}$ .

A second source electrode 114 such as Al is formed on the first source electrode 112 and the second insulating film 113 which is formed on the first source electrode 112. The second  
25 gate wiring 110 and the second source electrode 114 are arranged with a gap 110a between them. The second source electrode 114 is formed thicker than the first source electrode 112 on the N-type source region 108.

Deterioration such as deformation in an interface between  
30 different kinds of materials and an increase in resistance can be prevented by forming the first source electrode 112 and the second source electrode 114 out of the same conductive material.

Moreover, in this embodiment, an upper surface of the second source electrode 114 is formed higher than an upper surface of  
35 the second gate wiring 110. The upper surface of the second source electrode 114 may be on the same level with the upper surface of the second insulating film 113 on the second gate wiring 110.

However, it is preferable that the upper surface of the second source electrode 114 be formed higher than the upper surface of the second insulating film 113 on the second gate wiring 110.

5 A strap 115 which connects with the second source electrode 114 is formed on the second source electrode 114. The strap 115 is a connecting plate, for example, made of Al. The strap 115 is connected, for example, to a lead frame (not shown) for connection to the outside.

10 Next, a method of manufacturing a first lead-out wiring region including the gate wiring of the semiconductor device described in this embodiment will be explained by Fig. 2 to Fig. 7.

15 Thermal diffusion is performed, for example, by selectively ion-implanting an N-type impurity in the surface of a P-type base region 202 formed on an N-type semiconductor substrate 201 to thereby form an N-type source region (not shown) in a predetermined region of the cell forming region. Then, as shown in Fig. 2, a first insulating film 203 is formed on the P-type base region 202. A first gate wiring 204 is formed using a conductive material  
20 such as polysilicon on part of the first insulating film 203. The first gate wiring 204 is connected to a trench gate electrode (not shown) formed in the cell forming region such as a trench MOSFET. A first interlayer dielectric 205 is formed on a side surface and an upper surface of the first gate wiring 204 on the  
25 first insulating film 203.

Subsequently, a slot portion is formed in the first interlayer dielectric 205 such that the upper surface of the first gate wiring 204 is exposed. Then, a second gate wiring 206 is formed to fill at least the slot portion and electrically connected  
30 to the first gate wiring 204. The second gate wiring 206 is formed of a conductive material such as Al and used as a lead-out wiring. A first source electrode 207 is then formed on the P-type base region 202 and the N-type source region (not shown).

35 Thereafter, as shown in Fig. 3, a second insulating film 208 such as a silicon oxide film or a silicon nitride film is formed in such a manner as to cover part of the first source electrode 207 and an upper surface and a side surface of the second gate

wiring 206.

Then, as shown in Fig. 4, a resist film 209 is applied onto the second insulating film 208 and patterned, so that a pattern of the second insulating film 208 is formed on the second gate wiring 206 and the first interlayer dielectric 205.

Subsequently, as shown in Fig. 5, the resist film 209 is ashed, and a second source electrode 210 is formed on an exposed part of the first source electrode 207 and on the second insulating film 208.

Next, as shown in Fig. 6, the second source electrode 210 is etched, and a gap 206a is formed such that the second insulating film 208 on the second gate wiring 206 and part of the second insulating film 208 on the first source electrode 208 are exposed. An upper surface of the second source electrode 210 is formed higher than the upper surface of the second gate wiring 206.

Then, as shown in Fig. 7, a strap 211 is directly connected onto the second source electrode 210. The connection is made by ultrasonic bonding. The strap 211 is formed of Al, for example.

Fig. 8 shows a plan view of the semiconductor device of this embodiment. Here, 801 denotes a semiconductor substrate, 802 denotes a lead frame, 803 denotes a strap, 804 denotes a gate wire, and 805 denotes a gate wiring. 806 denotes an application region of ultrasonic waves. Fig. 9 is a fragmentary sectional view showing an outline of a section taken along the line C-C' in Fig. 8.

Since the upper surface of the source electrode is formed higher than the upper surface of the gate wiring as described above, it becomes possible to reduce shock applied to the insulating film formed on the gate wiring when the strap is connected to the source electrode by ultrasonic bonding. Namely, the following situation can be prevented: the gate wiring is crushed and deformed to the source electrode side to thereby cause a short-circuit between the gate wiring and the source electrode; or the insulating film formed on the gate wiring deteriorates to thereby cause a short-circuit between the strap and the gate wiring, and as a result, it becomes possible to eliminate a short-circuit fault without incurring an increase in internal resistance.

Although the aforementioned second source electrode is formed thicker than the first source electrode on the N-type source region, but it is not limited to this particular example. When the strap is connected onto the second source electrode, more  
5 force is applied to the electrode which is formed thicker as a cushioning material to absorb shock. If the first source electrode is formed thicker, the first source electrode functions as a cushioning material when the strap is connected onto the second source electrode. Accordingly, force is applied onto the first  
10 source electrode and also to the insulating film on the side wall of the gate wiring, which causes the deterioration of the insulating film. Hence, it is preferable to form the second source electrode thicker since more shock is absorbed by the second source electrode so that the possibility of deterioration of the second insulating  
15 film due to shock when the strap is connected is low.

Moreover, since the second source electrode is formed apart from the gate wiring with a gap therebetween, a short-circuit fault, which is caused because shock is particularly applied to an end portion of the second source electrode when the strap is  
20 connected to the upper portion thereof and thereby the second source electrode is deformed, can be prevented.

Furthermore, the second insulating film needs to be formed so as to cover the gate wiring, but by forming the insulating film to extend onto part of the upper surface of the first source  
25 electrode so that an end portion of the first source electrode is covered with the insulating film, a fault caused by misalignment in patterning can be prevented, and in addition, a short-circuit fault caused by deformation when shock is applied to the end portion of the first source electrode when the strap is connected to the  
30 upper portion can be prevented.

In this embodiment, the semiconductor device with an offset mesh trench structure in which a trench is formed in a mesh pattern is described, but without being limited to this, a semiconductor device with a stripe trench structure in which a trench is formed  
35 in a striped pattern is also possible.

(Second Embodiment)

Next, a semiconductor device of the second embodiment will be explained referring to Fig. 10.

In this embodiment, the explanation is given with an MOSFET and an IGBT as its examples. Fig. 10 is a fragmentary sectional  
5 view of a semiconductor device. As shown in Fig. 10, a first insulating film 1003 is formed, for example, on a P-type base region 1002 of a lead-out wiring region formed on an N-type semiconductor substrate 1001. A first gate wiring 1004 is formed on the first insulating film 1003.

10 A trench (not shown) is formed perpendicular to the first gate wiring 1004 in the P-type base region 1002 of a cell forming region. The trench has a stripe trench structure. An N-type source region 1005 is selectively formed on the surface of the P-type base region 1002 around the trench. Incidentally, Fig.  
15 10 is a fragmentary sectional view on the N-type source region 1005. The structure of the cell forming region not shown is the same as that in the aforementioned first embodiment, and hence the explanation thereof is omitted.

The first gate wiring 1004 is formed of a conductive material  
20 such as polysilicon and electrically connected to trench gate electrodes of the cell forming regions in other regions (not shown), respectively. A first interlayer dielectric 1006 such as an UDO or a BPSG is formed on a side surface and part of an upper surface of the first gate wiring 1004. A second gate wiring 1007 made  
25 of a conductive material such as Al is formed on the first gate wiring 1004 on which the first interlayer dielectric 1006 is not formed, and used as a lead-out wiring for the first gate wiring 1004. The first interlayer dielectric may be integrally formed by an insulating film made of the same material.

30 A first source electrode 1008 such as Al is formed on the N-type source region 1005, and the first source electrode 1008 is formed to be insulated from the first gate wiring 1004 by the first interlayer dielectric 1006.

On part of an upper surface of the first source electrode  
35 1008 and a side surface and an upper surface of the second gate wiring 1007, a second insulating film 1009 is formed to prevent a short-circuit between the second gate wiring 1007 and a strap

and a short-circuit between the first source electrode 1008 and the second gate wiring 1007 when the strap is connected by ultrasonic bonding.

Although the second insulating film 1009 is formed on part  
5 of the upper surface of the first source electrode 1008, it may not be formed thereon. By forming the insulating film to extend onto part of the upper surface of the first source electrode 1008 as described above, a short circuit fault caused by misalignment in patterning can be prevented, whereby a device with high yield  
10 and high reliability can be manufactured. The second insulating film 1009 is composed of a silicon oxide film, a silicon nitride film, or a stacked film thereof. It is desirable to use an insulating film with a certain degree of hardness as the second insulating film 1009 since an electrode layer is formed thereon.  
15 The thickness of the second insulating film 1009 is preferably 2  $\mu\text{m}$  to 4  $\mu\text{m}$ .

A second source electrode 1010 such as Al is formed on the first source electrode 1008 and the second insulating film 1009. The second source electrode 1010 is formed thicker than the first  
20 source electrode 1008 on the N-type source region 1005.

Deterioration such as deformation in an interface between different kinds of materials and an increase in resistance can be prevented by forming the first source electrode 1008 and the second source electrode 1010 with the same conductive material.

25 The second source electrode 1010 is formed also on the second insulating film 1009 formed on the gate wiring 1007. A strap 1011 which connects with the second source electrode 1010 is formed on the second source electrode 1010. The strap 1011 is a connecting plate, for example, made of Al. The strap 1011 is connected, for  
30 example, to a lead frame (not shown) for connection to the outside.

As described above, no gap is provided in the second source electrode in this embodiment. Accordingly, it becomes possible to reduce shock applied to the insulating film formed on the gate wiring when the strap is connected to the source electrode by  
35 ultrasonic bonding without the addition of steps. Namely, a short-circuit between the gate wiring and the source electrode due to the deformation of the gate wiring can be prevented, whereby



it becomes possible to eliminate a short-circuit fault without incurring an increase in internal resistance. Moreover, by forming the area of contact between the source electrode and the strap larger, a reduction in resistance becomes possible.

5           Although the aforementioned second source electrode is formed thicker than the first source electrode on the N-type source region, but the present invention is not limited to this particular example. When the strap is connected onto the second source electrode, more force is applied to the electrode which is formed  
10 thicker as a cushioning material to absorb shock. If the first source electrode is formed thicker, the first source electrode functions as a cushioning material when the strap is connected onto the second source electrode. Accordingly, force is applied onto the first source electrode and also to the insulating film  
15 on the side wall of the gate wiring, which causes the deterioration of the insulating film. Hence, it is preferable to form the second source electrode thicker since more shock is absorbed by the second source electrode so that the possibility of deterioration of the second insulating film due to shock when the strap is connected  
20 is low.

          Furthermore, the second insulating film needs to be formed so as to cover the gate wiring, but by forming the insulating film to extend onto part of the upper surface of the first source electrode so that an end portion of the first source electrode  
25 is covered with the insulating film, a fault caused by misalignment in patterning can be prevented, and in addition, a short-circuit fault caused by deformation when shock is applied to the end portion of the first source electrode when the strap is connected to the upper portion can be prevented.

30           In this embodiment, the semiconductor device with a stripe trench structure in which a trench is formed in a striped pattern is described, but without being limited to this, a semiconductor device with an offset mesh trench structure in which a trench is formed in a mesh pattern is also possible.

35           (Third Embodiment)

          A semiconductor device of the third embodiment will be explained referring to Fig. 11 to Fig. 19.

In this embodiment, the explanation is given with an MOSFET and an IGBT as its examples. Fig. 11 is a sectional view taken along the line A-A' - B-B' in Fig. 16. A first and second lead-out wiring regions and a cell forming region are shown. The first lead-out wiring region is a lead-out wiring region sandwiched between the cell forming regions, and the second lead-out wiring region is a lead-out wiring region formed in at least part of an outer peripheral region of the cell forming region.

As shown in Fig. 11, a P-type base region 1102 is formed, for example, on an N-type semiconductor substrate 1101 of the first lead-out wiring region and the cell forming region. First insulating films 1103a and 1103b are formed on the P-type base region 1102 of the first and second lead-out wiring regions and on the semiconductor substrate 1101. First gate wirings 1104a and 1104b are formed on the first insulating films 1103a and 1103b, respectively.

In the P-type base region 1102 of the cell forming region, a trench 1105 is formed perpendicular and parallel to the first gate wiring 1104a in the first lead-out wiring region. The trench 1105 has an offset mesh trench structure. Incidentally, Fig. 11 is a fragmentary sectional view of a region in which the trench 1105 is formed perpendicular to the first gate wiring 1104a in the first lead-out wiring region. A gate insulating film 1106 is formed in the trench 1105, and a trench gate electrode 1107 is buried in the trench 1105 in such a manner as to touch the gate insulating film 1106. An N-type source region 1108 is formed on the surface of the P-type base region 1102 around the trench 1105. The N-type source region 1108 is not formed around the trench 1105 on the first lead-out wiring region side.

A cell formed in the cell forming region functions as a MOSFET if an N<sup>+</sup>-type drain region is formed under the semiconductor substrate 1101 and a drain electrode is formed so as to touch the N<sup>+</sup>-type drain region, and functions as an IGBT (Insulated Gate Bipolar Transistor) if a P<sup>+</sup>-type collector region is formed under the semiconductor substrate 1101 and a collector electrode is formed so as to touch the P<sup>+</sup>-type collector region. The cell formed in the cell forming region is not limited to the above. The

structure of the cell is not limited to a trench type, and may be a planer type.

The first gate wirings 1104a and 1104b and the trench gate electrode 1107 are formed of a conductive material such as polysilicon and electrically connected to each other in another region (not shown).

First interlayer dielectrics 1109a and 1109b such as a UDO (Undoped Oxide) or a BPSG are formed on side surfaces and part of each of upper surfaces of the first gate wirings 1004a and 1104b of the first and second lead-out wiring regions, respectively. The first insulating films and the first interlayer dielectrics may be formed integrally by an insulating film made of the same material. On the first gate wirings 1104a and 1104b on which the first interlayer dielectrics 1109a and 1109b are not formed, second gate wirings 1110a and 1110b made of a conductive material such as Al are formed and used as lead-out wirings. A second interlayer dielectric 1111 is formed on the trench electrode 1107. The second interlayer dielectric 1111 may be completely buried in the trench 1105.

A first source electrode 1112 such as Al is formed on the P-type base region 1102 and the N-type source region 1108 of the cell forming region. The first source electrode 1112 is formed so as to have a large area, which leads to a reduction in resistance. The first source electrode 1112 is formed to be insulated from the first gate wirings 1104a and 1104b and the trench gate electrode 1107 by the first interlayer dielectrics 1109a and 1109b and the second interlayer dielectric 1111. Second insulating films 1113a and 1113b whose ends are formed on part of an upper surface of the first source electrode 1112 are formed on side surfaces and upper surfaces of the second gate wirings 1110a and 1110b, respectively. The second insulating film 1113a formed in the first lead-out wiring region is formed in order to, when an almost platy connecting plate (here called a strap) is connected to the upper portion thereof by ultrasonic bonding, prevent a short-circuit between the second gate wiring 1110a and the strap and a short-circuit between the first source electrode 1112 and the second gate wiring 1110a.

Although the second insulating films 1113a and 1113b are formed on part of the upper surface of the first source electrode 1112, they may not be formed thereon. However, by forming the insulating films to extend onto part of the upper surface of the first source electrode 1112 as described above, a short circuit fault caused by misalignment in patterning can be prevented, whereby a device with high yield and high reliability can be manufactured. The second insulating films 1113a and 1113b are composed of a silicon oxide film, a silicon nitride film, or a stacked film thereof. It is desirable to use an insulating film with a certain degree of hardness as the second insulating films 1113a and 1113b since an electrode layer is formed thereon. The thickness of the second insulating films 1113a and 1113b is preferably 2  $\mu\text{m}$  to 4  $\mu\text{m}$ .

A second source electrode 1114 such as Al is formed on the first source electrode 1112 in the cell forming region and on part of each of the second insulating films 1113a and 1113b which are formed on the first source electrode 112. An upper surface of the second source electrode 1114 is formed higher than upper surfaces of the second gate wirings 1110a and 1110b. The second gate wiring 1110a and the second source electrode 1114 in the first lead-out wiring region are arranged with a gap 1110c between them. The second source electrode 1114 is formed thicker than the first source electrode 1112 on the N-type source region 1108. Moreover, a gate electrode 1115 such as Al is formed on the second gate wiring 1110b in the second lead-out wiring region and on the second insulating film 1113b formed on the first source electrode 1112. The second source electrode and the gate electrode 1115 are formed apart from each other.

Deterioration such as deformation in an interface between different kinds of materials and an increase in resistance can be prevented by forming the first source electrode 1112 and the second source electrode 1114 with the same conductive material.

A strap 1116a which connects with the second source electrode 1114 is formed on the second source electrode 1114. The strap 1116a is a connecting plate, for example, made of Al. The strap 1116a is connected to a lead frame (not shown), for example, for

connection to the outside. A strap 1116b which connects with the gate electrode 1115 is formed on the gate electrode 1115. The strap 1116b is connected to the lead frame (not shown), for example, for connection to the outside. In a surface region of an outer peripheral edge of the second lead-out wiring region, an N-type stopper region 1117 is formed to prevent the extension of a depletion layer when a reverse bias is applied.

The example in which the strap 1116b as the connecting plate is connected to the gate electrode 1115 is described here, but, without being limited to this example, as shown in the first embodiment, connection by a gate wire is also possible.

Next, a method of manufacturing the first and second lead-out wiring regions including gate wirings of the semiconductor device shown in Fig. 11 which is described in this embodiment will be explained by Fig. 12 to Fig. 15. The cell forming region, part of which is omitted, will be described.

As shown in Fig. 12, a P-type base region 1202 is formed on a semiconductor substrate 1201 in the first lead-out wiring region. Subsequently, first insulating films 1203a and 1203b are formed on the P-type base region 1202 in the first and second lead-out wiring regions and on the semiconductor substrate 1201. Polysilicon is deposited on the first insulating films 1203a and 1203b and etched to form first gate wirings 1204a and 1204b on part of each of the first insulating films 1203a and 1203b in the first and second lead-out wiring regions. Silicon nitride films are formed on upper surfaces and side surfaces of the first gate wirings 1204a and 1204b and etched to form slot portions such that part of each of the upper surfaces of the first gate wirings 1204a and 1204b is exposed, and thus interlayer dielectrics 1205a and 1205b are formed.

In the cell forming region, a cell at least composed of a gate insulating film 1206, a trench gate electrode 1207, an N-type source region 1208, and a second interlayer dielectric 1209 is formed. Then, Al is deposited and etched to form second gate wirings 1210a and 1210b in the first and second lead-out wiring regions, respectively, and a first source electrode 1211 is formed in the cell forming region. An N-type stopper region

1212 is formed in a surface region of an outer peripheral edge of the second lead-out wiring region.

Thereafter, as shown in Fig. 13, a second insulating film 1213 such as a silicon oxide film or a silicon nitride film is deposited in the first and second lead-out wiring regions.

Then, as shown in Fig. 14, by applying a resist film and forming a resist pattern, a second insulating film 1213a such as covers the second gate wiring 1210a and a second insulating film 1213b such that part of an upper surface of the second gate wiring 1210b is exposed are formed. The resist pattern is removed by ashing. End portions of the second insulating films 1213a and 1213b are formed to extend onto the first source electrode 1211.

Next, as shown in Fig. 15, by depositing Al, applying a resist film onto the Al, and forming a resist pattern, a second source electrode 1214 is formed on the first source electrode 1211 and on the insulating films 1213a and 1213b on the first source electrode 1211. A gate electrode 1215 is formed on the second wiring 1210b and the second insulating film 1213b formed in the second lead-out wiring region. An end portion of the gate electrode 1215 is formed to extend onto the second insulating film 1213b formed on the first source electrode 1211.

The second insulating film 1213b is formed so that part of an upper surface of the second gate wiring 1210b is exposed, and out of the second insulating film 1213b, a portion which is formed on the opposite side of the second insulating film extending onto the first source may be a film with a lower hardness than a silicon nitride film and a silicon oxide film and hence may be formed of polyimide used as a protective film since it is unnecessary to form an electrode thereon. Subsequently, a strap 1216a is formed on the cell forming region and the first lead-out wiring region by ultrasonic bonding, while a strap 1216b is formed on the gate electrode formed in the second lead-out wiring region by ultrasonic bonding and connected to the lead frame (not shown).

Fig. 16 shows a plan view of the semiconductor device of this embodiment. Here, 1601 denotes a semiconductor substrate, 1602 denotes a lead frame, 1603 denotes a strap, 1604a denotes a gate wiring in the first lead-out wiring region, and 1604b denotes

a gate wiring in the second lead-out wiring region. 1605 denotes an application region of ultrasonic waves. A fragmentary sectional view showing an outline of a section taken along the line C-C' in Fig. 16 is the same as Fig. 9 shown in the first embodiment.

Since an upper surface of the second source electrode is formed higher than or on about the same level with an upper surface of the insulating film on the gate wiring as described above, it becomes possible to reduce shock applied to the insulating film formed on the gate wiring when the strap is connected to the source electrode by ultrasonic bonding. Namely, the following situation can be prevented: the gate wiring is crushed and deformed to the source electrode side to thereby cause a short-circuit between the gate wiring and the source electrode; or the insulating film formed on the gate wiring deteriorates to thereby cause a short-circuit between the strap and the gate wiring, whereby it becomes possible to eliminate a short-circuit fault without incurring an increase in internal resistance.

Although the aforementioned second source electrode is formed thicker than the first source electrode on the N-type source region, but the present invention is not limited to this particular example. When the strap is connected onto the second source electrode, more force is applied to the electrode which is formed thicker as a cushioning material to absorb shock. If the first source electrode is formed thicker, the first source electrode functions as a cushioning material when the strap is connected onto the second source electrode. Accordingly, force is applied onto the first source electrode and also to the insulating film on the side wall of the gate wiring, which causes the deterioration of the insulating film. Hence, it is preferable to form the second source electrode thicker since more shock is absorbed by the second source electrode so that the possibility of deterioration of the second insulating film due to shock when the strap is connected is low.

Moreover, since the second source electrode is formed apart from the gate wiring with a gap therebetween, a short-circuit fault, which is caused because shock is particularly applied to

an end portion of the second source electrode when the strap is connected to the upper portion thereof and thereby the second source electrode is deformed, can be prevented.

Furthermore, although the second insulating film formed  
5 in the first lead-out wiring region is formed to extend onto part of the upper surface of the first source electrode, the second insulating film has only to be formed so as to cover the second gate wiring. However, by forming the second insulating film to extend onto part of the upper surface of the first source electrode  
10 so that an end portion of the first source electrode is covered with the second insulating film, a fault caused by misalignment in patterning can be prevented, and in addition, a short-circuit fault caused by deformation when shock is applied to the end portion of the first source electrode when the strap is connected to the  
15 upper portion can be prevented.

Moreover, in a related art, as shown in Fig. 25, a second lead-out wiring region which is formed in the same process as a first lead-out wiring region is formed side by side with a cell forming region, and no cell such as a MOSFET is formed under the  
20 second lead-out wiring region. As shown in Fig. 26A and Fig. 26B, in semiconductor chips corresponding to packages having symmetrical structures, the positions of respective gate electrodes 2602 on respective semiconductor chips 2601 are different even in the packages of the same size, whereby there  
25 is a problem that the semiconductor chips 2601 to be mounted need to be designed individually. Here in Fig. 26A and Fig. 26B, 2603 denotes a source electrode, and 2604 denotes a gate wiring.

Besides, there is a problem that when, in order to reduce on-state resistance, the area of the cell forming region of the  
30 semiconductor chip is formed wider, the number of cells is increased, and the area of the source electrode is formed more widely, the area, number, position, shape, and so on of gate electrodes are limited. Further, there is a problem that it is necessary to select the area, number, position, shape, and so on of gate electrodes  
35 depending on the position of a lead frame.

In this embodiment, in the second lead-out wiring region, the second insulating film is formed between the gate electrode



and the first source electrode, and they are insulated. Hence, the cell forming region can be provided under part of the second lead-out wiring region, whereby regardless of the area of the gate electrode, the area of the cell forming region can be formed more widely, resulting in a reduction in on-state resistance. Moreover, regardless of the area of the cell forming region and the position of the lead frame, the area, number, position, shape, and so on of gate electrodes can be selected. Namely, desired area, number, position, shape, and so on of gate electrodes can be selected, and in addition, the area of the cell forming region can be formed more widely, leading to a reduction in on-state resistance.

Furthermore, concurrently with the formation of the wider cell forming region, the gate electrodes can be formed in two corner portions of the semiconductor chip as shown in Fig. 17, and hence new designing is unnecessary even in semiconductor chips (for example, in Fig. 26A and Fig. 26B) in which the positions of gate electrodes are different corresponding to packages. 1701 denotes a semiconductor chip, 1702 denotes a gate electrode, 1703 denotes a source electrode, and 1704 denotes a gate wiring.

Moreover, by forming the gate electrode in a region parallel to a long side or a short side of the semiconductor chip as shown in Fig. 18A and Fig. 18B, it is possible not only to form the cell forming region widely but also to form the gate electrode optionally widely. Thanks to this formation, the strap structure can be formed more easily, and besides a reduction in resistance becomes possible. Further, since the connection between the gate electrode and the lead frame can be performed at an optional position, the semiconductor device with a high degree of flexibility in position, size, and so on can be formed.

The second insulating film in the first lead-out wiring region and the second insulating film in the second lead-out wiring region can be formed in the same process. Also, the second source electrode in the cell forming region and the gate electrode in the second lead-out wiring region can be formed in the same process.

Although the semiconductor device with an offset mesh trench structure in which a trench is formed in a mesh pattern is described

in this embodiment, the present invention is not limited to this example, and a semiconductor device with a stripe trench structure in which a trench is formed in a striped pattern is also possible. Moreover, although, in this embodiment, as the structure of the first lead-out wiring region, the first embodiment (Fig. 1) in which the source electrode is not formed on the second gate wiring is used as shown in Fig. 11, the second embodiment (Fig. 10) in which the source electrode is formed on the second gate wiring as shown in Fig. 19 can be also used.

In the aforementioned first to third embodiments, a fault due to shock caused when the strap is bonded by ultrasonic bonding is described, but the present invention is not limited to this and has also a sufficient effect on shock caused by pressure welding bonding.

Moreover, the example in which the source electrode is composed of a double-layer electrode layer is described, but it may be composed of a one-layer electrode layer or a three or more layer electrode. Further, although the case where the source electrode is formed on the source region is explained, the source electrode may be a drain electrode, an emitter electrode, a collector electrode, or the like depending on the structure of a cell formed in the cell forming region.